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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,313	04/12/2000	Hidehiko Kira	000452	6169

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EXAMINER	
RENNER, CRAIG A	

ART UNIT	PAPER NUMBER
2652	24

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/548,313	KIRA ET AL.	
	Examiner	Art Unit	
	Craig A. Renner	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-37* is/are pending in the application.

4a) Of the above claim(s) *4,6,9-29,31 and 32* is/are withdrawn from consideration.

5)☒ Claim(s) *36 and 37* is/are allowed.

6)☒ Claim(s) *1,2,5,8,30 and 33-35* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 14-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to one or more non-elected inventions/species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7, filed 4 February 2002.

2. Claims 10-13 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to one or more non-elected inventions/species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 9, filed 14 March 2002.

3. Claims 4, 6, 9 and 31-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to one or more non-elected inventions/species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 14, filed 7 November 2002.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5, 8, 30 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraishi et al. (US 6,084,746) in view of Mones et al. (US 4,173,907).

With respect to claims 1-~~3~~2, 5, 30 and 34, Shiraishi teaches a head assembly (17) comprising a mounting surface (31); an integrated circuit chip (20) which is mounted on the mounting surface (as shown in FIGS. 3-4, for instance) and processes signals, and a head slider (19) which is provided with a head (line 10 in column 6, for instance) and is mounted on the mounting surface (as shown in FIGS. 3-4, for instance), a height (H1) of the integrated circuit chip being lower than a height (H2) of the head slider from the mounting surface (as shown in FIG. 4, for instance) [as per claims 1-2, 5 and 30]; wherein the mounting surface is substantially flat (as shown in FIGS. 3-4, for instance) [as per claim 34].

With respect to claims 8 and 35, Shiraishi teaches a disk unit (FIG. 1, for instance) for reading information from and writing information to a disk (10), comprising a head assembly (17) having a mounting surface (31), a head slider (19) provided with a head (line 10 in column 6, for instance) and mounted on the mounting surface (as shown in FIGS. 3-4, for instance), and an integrated circuit chip (20) which is mounted on the mounting surface (as shown in FIGS. 3-4, for instance) and processes information read from and/or written to the disk via the head, a height (H1) of the integrated circuit chip being lower than a height (H2) of the head slider from the

mounting surface (as shown in FIG. 4, for instance) [as per claim 8]; wherein the mounting surface is substantially flat (as shown in FIGS. 3-4, for instance) [as per claim 35].

With respect to claim 33, Shiraishi teaches a unit (FIG. 1, for instance) for reading information from and writing information to a recording medium (10), comprising a head assembly (17) having a mounting surface (31), a head slider (19) provided with a head (line 10 in column 6, for instance) and mounted on the mounting surface (as shown in FIGS. 3-4, for instance), and an integrated circuit chip (20) which is mounted on the mounting surface (as shown in FIGS. 3-4, for instance) and processes information read from and/or written to the recording medium via the head, a height (H1) of the integrated circuit chip being lower than a height (H2) of the head slider from the mounting surface (as shown in FIG. 4, for instance).

As the claims are directed to head assembly, per se, the method limitation appearing in line 2 of claim 2 can only be accorded weight to the extent that it affects the structure of the completed head assembly. Note that "[d]etermination of patentability in 'product-by-process' claims is based on product itself, even though such claims are limited and defined by process [i.e., "evaporation"], and thus product in such claim is unpatentable if it is the same as, or obvious form, product of prior art, even if prior product was made by a different process", *In re Thorpe, et al.*, 227 USPQ 964 (CAFC 1985). Furthermore, note that a "[p]roduct-by-process claim, although reciting subject matter of claim in terms of how it is made [i.e., "evaporation"], is still product claim; it is patentability of product claimed and not recited process steps that must be

established, in spite of fact that claim may recite only process limitations", *In re Hirao and Sato*, 190 USPQ 685 (CCPA 1976).

Shiraishi, however, remains silent as to the integrated circuit chip height further including a "layer 2μm or thinner" as per claims 1-2, 5, 8, 30 and 33-35, "wherein said layer covers at lest peripheral portions of the integrated circuit chip" as per claim 5, and "wherein said layer covers at least an entire upper surface of the integrated circuit chip" as per claim 30.

Mones teaches an integrated circuit chip height further including a layer 2μm or thinner (lines 51-54 in column 1, for instance, i.e., "1 to 3 microns" includes the range 1-2μm), wherein the layer covers at least peripheral portions of an integrated circuit chip (lines 51-54 in column 1, for instance, i.e., "the upper surface" includes peripheral portions of the upper surface) and wherein the layer covers at least an entire upper surface of the integrated circuit chip (lines 51-54 in column 1, for instance, i.e., "the upper surface" includes an entire upper surface) for the purpose of protecting the chip during handling thereof. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have had the integrated circuit chip height of Shiraishi further include a layer 2μm or thinner, wherein the layer covers at least peripheral portions of the integrated circuit chip and wherein the layer covers at least an entire upper surface of the integrated circuit chip, as taught by Mones. The rationale is as follows:

One of ordinary skill in the art would have been motivated to have had the integrated circuit chip height of Shiraishi further include a layer 2μm or thinner, wherein

the layer covers at least peripheral portions of the integrated circuit chip and wherein the layer covers at least an entire upper surface of the integrated circuit chip, as taught by Mones, since such protects the chip during handling thereof.

Allowable Subject Matter

6. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 36-37 are allowable over the prior art of record.

Response to Arguments

7. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig A. Renner whose telephone number is (703) 308-0559. The examiner can normally be reached on Tuesday-Friday 7:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T. Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig A. Renner
Primary Examiner
Art Unit 2652

CAR